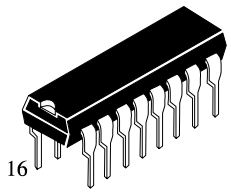
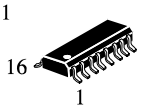
IN74AC192

Presettable BCD/Decade UP/DOWN Counter

High-Speed Silicon-Gate CMOS



N SUFFIX
PLASTIC



D SUFFIX
SOIC

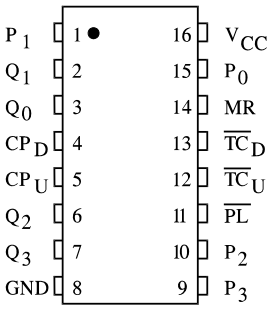
ORDERING INFORMATION
IN74AC192N Plastic
IN74AC192D SOIC
T_A = -40° to 85° C for all packages

The IN74AC192 is identical in pinout to the LS/ALS192, HC/HCT192. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

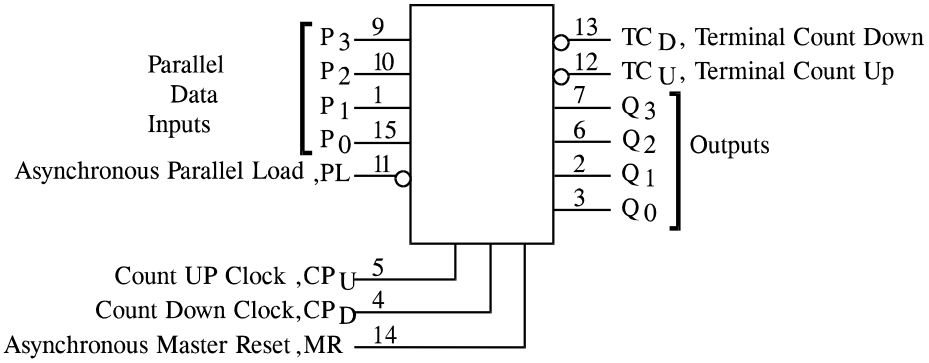
The counter has two separate clock inputs, a Count Up Clock and Count Down Clock inputs. The direction of counting is determined by which input is clocked. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. This counter may be preset by entering the desired data on the P0, P1, P2, P3 input. When the Parallel Load input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as devide-by-n by modifying the count lenght with the preset inputs. In addition the counter can also be cleared. This is accomplished by inputting a high on the Master Reset input. All 4 internal stages are set to low independently of either clock input.Both a Terminal Count Down (TC_D) and Terminal Count Up (TC_U) Outputs are provided to enable cascading of both up and down counting functions. The TC_D output produces a negative going pulse when the counter underflows and TC_U outputs a pulse when the counter overflows. The counter can be cascaded by connecting the TC_U and TC_D outputs of one device to the Count Up Clock and Count Down Clock inputs, respectively, of the next device.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA, 0.1 µA @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Temperature, All Package Types		-40	+85	°C
I_{OH}	Output Current - High			-24	mA
I_{OL}	Output Current - Low			24	mA
t_r, t_f	Input Rise and Fall Time *	V_{CC} =3.0 V	0	150	ns/V
	(except Schmitt Inputs)	V_{CC} =4.5 V	0	40	
		V_{CC} =5.5 V	0	25	

* V_{IN} from 30% to 70% V_{CC}

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits 25 °C	Guaranteed Limits -40°C to 85°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High-Level Output Voltage	$I_{OUT} \leq$ -50 µA	3.0 4.5 5.5	2.9 4.4 5.4	2.9 4.4 5.4	V
		*V_{IN}=V_{IH} or V_{IL} I_{OH}=-12 mA I_{OH}=-24 mA I_{OH}=-24 mA	 3.0 4.5 5.5	 2.56 3.86 4.86	 2.46 3.76 4.76	
V_{OL}	Maximum Low-Level Output Voltage	$I_{OUT} \leq$ 50 µA	3.0 4.5 5.5	0.1 0.1 0.1	0.1 0.1 0.1	V
		*V_{IN}=V_{IH} or V_{IL} I_{OL}=12 mA I_{OL}=24 mA I_{OL}=24 mA	 3.0 4.5 5.5	 0.36 0.36 0.36	 0.44 0.44 0.44	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	µA
I_{OLD}	+Minimum Dynamic Output Current	V_{OLD}=1.65 V Max	5.5		75	mA
I_{OHD}	+Minimum Dynamic Output Current	V_{OHD}=3.85 V Min	5.5		-75	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND	5.5	8.0	80	µA

* All outputs loaded; thresholds on input associated with output under test.
+Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}

FUNCTION TABLE

Inputs MR	Inputs $\overline{PL}$	Inputs CP_U	Inputs CP_D	Mode
H	X	X	X	Reset(Asyn.)
L	L	X	X	Preset(Asyn.)
L	H	↓	H	No Count
L	H	↑	H	Count Up
L	H	H	↓	Count Down
L	H	H	↑	No Count

X = don't care

The IN74AC192 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will follow the sequence 10, 11, 6: 12, 13, 4: 14, 15, 2 if counting Up, and follow the sequence 15, 14, 13, 12, 11, 10, 9 if counting Down.

Logic equations
For Terminal Count:

$\overline{TC_U} = Q_0 \bullet Q_3 \bullet \overline{CP_U}$

$\overline{TC_D} = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limits				Unit
			25 °C		-40°C to 85°C		
			Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (Figure 1)	3.3 5.0	88 120		40 55		MHz
t_{PLH}	Propagation Delay, CP_U or CP_D to $\overline{TC_U}$ or TC_D (Figure 2)	3.3 5.0		20 13		22 14.5	ns
t_{PHL}	Propagation Delay, CP_U or CP_D to $\overline{TC_U}$ or TC_D (Figure 2)	3.3 5.0		19 11.5		21 13.0	ns
t_{PLH}	Propagation Delay, CP_U or CP_D to Q_n (Figure 1)	3.3 5.0		15 10		17.0 11.5	ns
t_{PHL}	Propagation Delay, CP_U or CP_D to Q_n (Figure 1)	3.3 5.0		15 9.5		17.0 11	ns
t_{PLH}	Propagation Delay, P_n to Q_n (Figure 3)	3.3 5.0		15 10		17.0 11.5	ns
t_{PHL}	Propagation Delay, P_n to Q_n (Figure 3)	3.3 5.0		15 9.5		17.0 11	ns
t_{PLH}	Propagation Delay, $\overline{PL}$ to Q_n (Figure 4)	3.3 5.0		15 10		17 11.5	ns
t_{PHL}	Propagation Delay, $\overline{PL}$ to Q_n (Figure 4)	3.3 5.0		20 12.5		22 14	ns
t_{PHL}	Propagation Delay, MR to Q_n (Figure 5)	3.3 5.0		20 12.5		22 14	ns
t_{PLH}	Propagation Delay, MR to $\overline{TC_U}$ (Figure 6)	3.3 5.0		18 12		20 13.5	ns
t_{PHL}	Propagation Delay, MR to $\overline{TC_D}$ (Figure 6)	3.3 5.0		19 11.5		21 13.0	ns
t_{PLH}	Propagation Delay, $\overline{PL}$ to $\overline{TC_U}$ or $\overline{TC_D}$ (Figure 6)	3.3 5.0		20 13		22 14.5	ns
t_{PHL}	Propagation Delay, $\overline{PL}$ to $\overline{TC_U}$ or $\overline{TC_D}$ (Figure 6)	3.3 5.0		15 8.5		17 10	ns
t_{PLH}	Propagation Delay, P_n to $\overline{TC_U}$ or $\overline{TC_D}$ (Figure 6)	3.3 5.0		20 13		22 14.5	ns
t_{PHL}	Propagation Delay, P_n to $\overline{TC_U}$ or $\overline{TC_D}$ (Figure 6)	3.3 5.0		20 12.5		22 14	ns
C_{IN}	Maximum Input Capacitance	5.0	4.5		4.5		pF

		Typical @25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance	45	pF

*Voltage Range 3.3 V is 3.3 V ±0.3 V
Voltage Range 5.0 V is 5.0 V ±0.5 V

TIMING REQUIREMENTS(C_L=50pF, Input t_r=t_f=3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limits 25 °C	Guaranteed Limits -40°C to 85°C	Unit
t_{su}	Minimum Setup Time, P_n to $\overline{PL}$ (Figure 7)	3.3 5.0	9 6	10 7	ns
t_h	Minimum Hold Time, $\overline{PL}$ to P_n (Figure 7)	3.3 5.0	-1.0 -1.0	0 0	ns
t_w	Minimum Pulse Width, $\overline{PL}$ (Figure 4)	3.3 5.0	17 12	21 13	ns
t_w	Minimum Pulse Width, CP_U or CP_D (Figure 1)	3.3 5.0	11 8	12 9	ns
t_w	Minimum Pulse Width, MR (Figure 5)	3.3 5.0	14 10	16 12	ns
t_{rec}	Minimum Recovery Time, $\overline{PL}$ to CP_U or CP_D (Figure 5)	3.3 5.0	9 12	10 13	ns
t_{rec}	Minimum Recovery Time, MR to CP_U or CP_D (Figure 5)	3.3 5.0	17 12	21 14	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V
Voltage Range 5.0 V is 5.0 V ±0.5 V

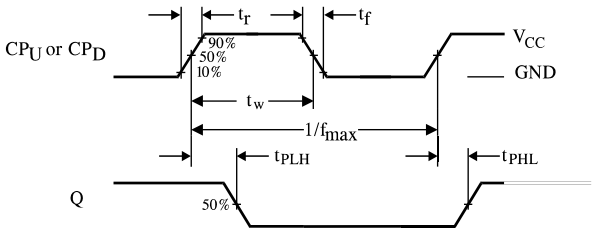


Figure 1. Switching Waveforms

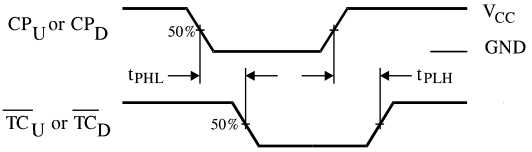


Figure 2. Switching Waveforms

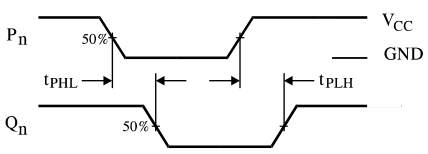


Figure 3. Switching Waveforms

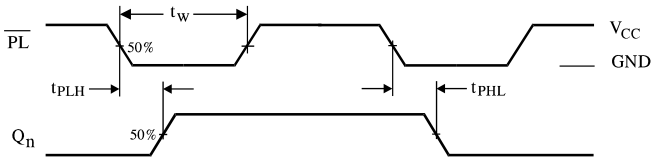


Figure 4. Switching Waveforms

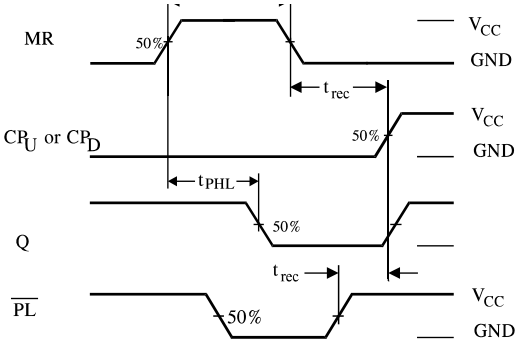


Figure 5. Switching Waveforms

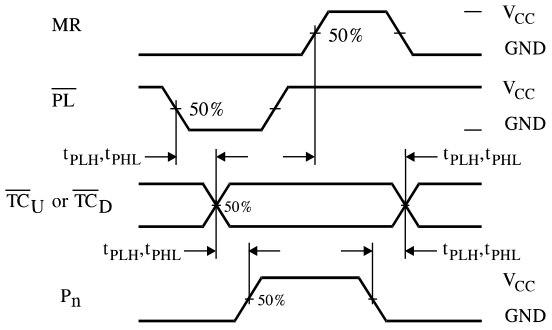


Figure 6. Switching Waveforms

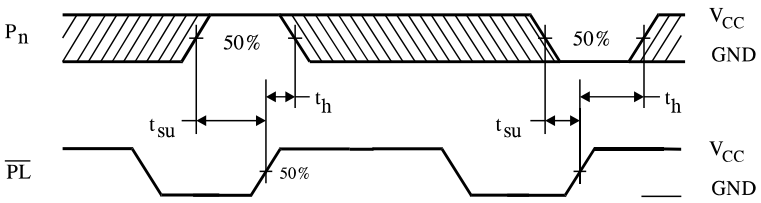
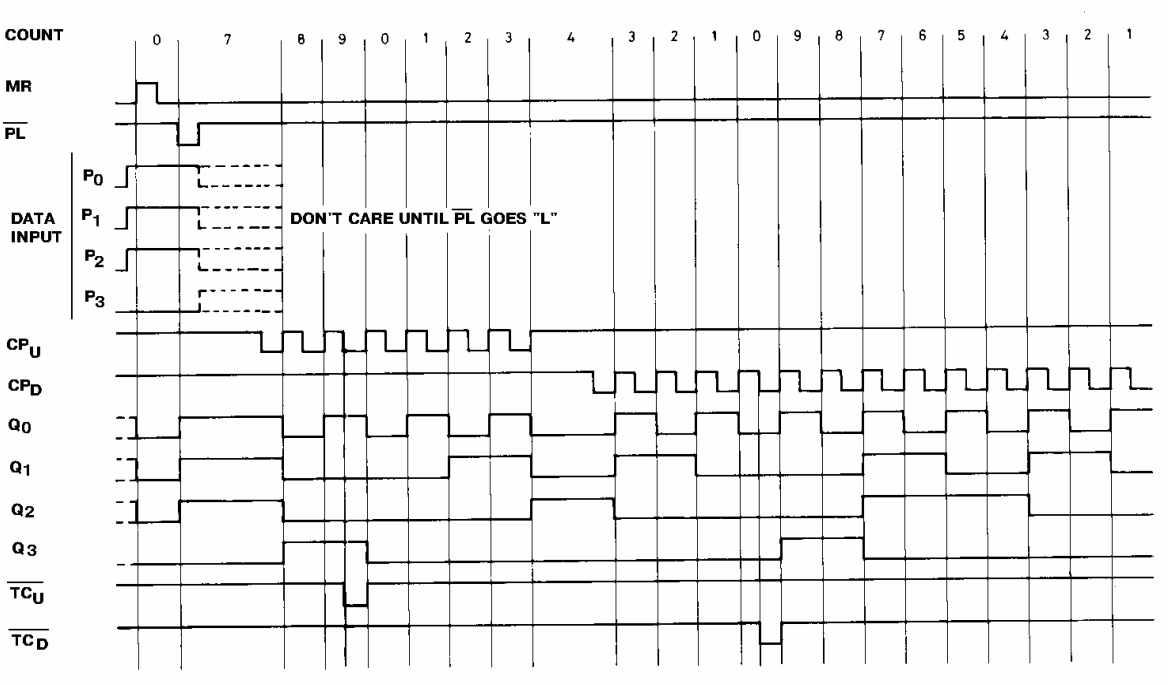


Figure 7. Switching Waveforms

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM